Amendment to the Specification:

Please amend the paragraph beginning on page 12, line 4, as follows:

Fig. 8 provides details of a data receiver interface for a CMTS, in accordance with the present invention. The Block Segment Converter, or Frequency Stacker 805, permits optimal use of the invention, by enabling presentation of a contiguous upstream spectrum to the data receiver banks 810. The stacker 805 efficiently organizes otherwise unrelated multiple channels into a densely packed spectrum on a single cable, which can be subsequently coupled to the ADC via an associated single connector.

Please amend the paragraph beginning on page 12, line 12, as follows:

Fig. 9 shows the internal architecture of a 4D x 16U module 900 used in a CMTS line card, in accordance with the present invention. Fig. 10 shows details of the receiver block ~~250~~ 910 used multiple times in the receiver bank ~~200~~ 900 of Fig. 9.

Please amend the paragraph beginning on page 12, line 17, as follows:

Fig. 11 shows a prior art FIR digital filter that is used in an illustrative embodiment for the digital filter block 1010 of Fig. 10. The digital filter chosen is an Optimum Equiripple Linear-Phase FIR Filter. A Chebyshev approximation is used, wherein the weighted approximation error between the desired frequency response and the actual frequency response is spread evenly across the passband and evenly across the stopband of the filter minimizing the maximum error. The resulting filter designs have ripples in both the passband and the stopband. The specific approximation used is the Parks-McClellan Alternation theorem.

Please amend the paragraph beginning on page 13, line 1, as follows:

Prototype lowpass filters are designed for each desired bandwidth. Fig. 12 shows the bandwidths and accompanying symbol and bit rates that may be obtained through the programmable provisioning of the digital filter block 1010 of Fig. 10. The coefficients for a DC center frequency are computed for each desired bandwidth using a Parks-McClellan program employing the Remez exchange algorithm (or the Rabiner variation), as decribed in section 8.2.4 of the Proakis and Manolakis text. The Parks-McClellan program is executed or interpreted using any numerical analysis application suite, including preferred applications such as MATLAB or Mathmatica.

Please amend the paragraph beginning on page 13, line 17, as follows:

Fig. 13 is a flow chart describing the (re)provisioning (block 1305) of the digital filter block 1010 within a selected one of the receivers 910 of Fig 9. The operational coefficients are generated in the field during provisioning from the corresponding DC coefficients (block 1310). The DC coefficients for the prototype lowpass filter, corresponding to the desired bandpass bandwidth, are retrieved from the non-volatile storage (block 1315) and are used to generate the operational coefficients in the field during provisioning. This field generation is done using the Bandpass Transformation described in section 8.4.2 of Proakis and Manolakis.

Please amend the paragraph beginning on page 14, line 2, as follows:

When a desired center frequency and bandpass bandwidth are selected for provisioning a particular receiver, the D.C. coefficients associated with the desired bandwidth are retrieved and subjected to a band-pass transformation (block 1320). The resulting operational coefficients are then loaded into coefficient latches in the digital filter for a selected receiver from the channel bank (block 1325).

Please amend the paragraph beginning on page 14, line 16, as follows:

Fig. 14 shows an illustrative embodiment of 4D x 16U module ~~100~~ 900 of Fig. 9, wherein four transmitter sub-modules ~~300~~ 915 and one receiver sub-module ~~200~~ 910 are implemented on a single integrated circuit 1405. In this illustrative 4D x 16U embodiment, there are downstream channels and 16 upstream channels. Four connectors 920 are required for the downstream channels and only a single connector 925 is required for all 16 upstream channels. The illustrative embodiment thus has **5** total connectors, compared to 20 total connectors in a comparable prior art system.

Please amend the paragraph beginning on page 14, line 24, as follows:

Fig. 15 shows another illustrative embodiment of the 4D x 16U module ~~100~~ 900 of Fig. 9, wherein 4 transmitter sub-modules ~~300~~ 915, one receiver sub-module ~~200~~ 910, the ADC ~~500~~ 930, and the non-volatile storage for the D.C. Coefficients ~~710~~ 940, are implemented on a single integrated circuit 1505. Fig. 16 shows a line card for a CMTS using multiple instances of the 4D x 16U module ~~100~~ 900 of Fig. 9.